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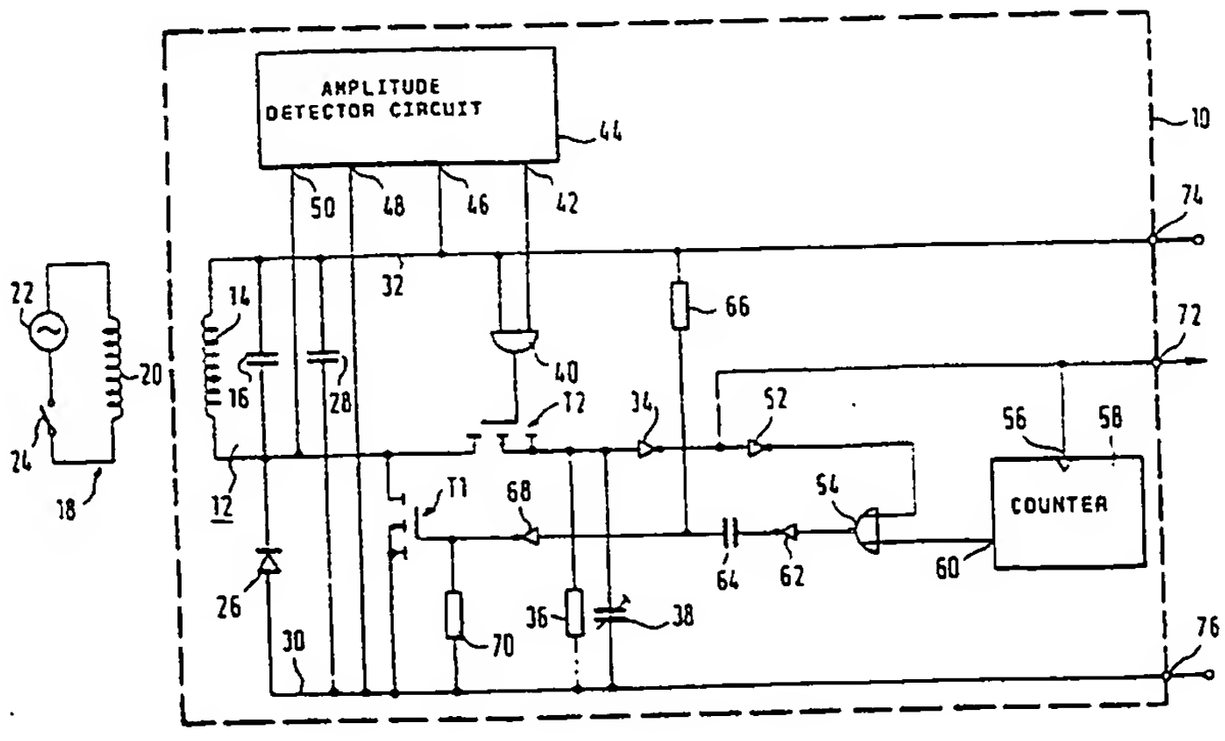
(54) circuit arrangement

(57) A circuit arrangement is described for generating pulses for maintaining the oscillations of a resonance circuit after termination of an outside stimulation of the oscillations by means of an HF carrier oscillation. The circuit arrangement comprises an energy storage element (28) chargeable by the HF carrier oscillation to a supply voltage value. An amplitude detector circuit (44) serves to generate a trigger circuit when the oscillation amplitude of the resonance circuit (12) drops beneath the supply voltage value. A first switching element (T2) supplies the oscillations of the resonance circuit (12) under the control of the trigger signal to a delay circuit (34, 52, 58, 54, 62, 68) which at its output furnishes switching pulses with a predetermined phase position with respect to the oscillations of the resonance circuit (12). A second switching element (T1), for the duration of each switching pulse, enables the supply of energy from the energy storage element (28) to the resonance circuit (12).

FIG.1



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the negator 34 and the ground line 30 there is a resistor 36 and a trimmer capacitor 38. Connected to the gate electrode of the MOS field-effect transistor T2 is the output of an AND circuit 40 which is connected with one input to the supply voltage line 32 and with the other input to an output 42 of an amplitude detector circuit 44. The amplitude detector circuit 44 also comprises an input 46 connected to the supply voltage line 32, an input 48 connected to the ground line 30 and an input 50 connected to the connection point between the resonance circuit 12 and the anode of the diode 26.

The output of the negator 34 is connected to the input of a further negator 52 of which the output is connected to an input of a NOR circuit 54. In addition the output of the negator 34 is connected to the counting input 56 of a counter 58 of which the output 60 is connected to the second input of the NOR circuit 54. The output of the NOR circuit is connected to the input of a further negator 62 which is connected to a terminal of a capacitor 64. The second terminal of the capacitor is in connection via a resistor 66 with the supply voltage line 32 and is moreover connected to the input of a negator 68 of which the output is connected to the gate electrode of the MOS field-effect transistor T1. Between the gate electrode of said MOS field-effect transistor T1 and the ground line 30 there is a resistor 70.

The circuit arrangement 10 operates as follows:

To enable the circuit arrangement 10 to become active and emit clock pulses at its output 72 the resonance circuit 12 must be stimulated to oscillate. This is done in that the switch 24 of the only schematically illustrated transmitter 18 is closed so that the HF carrier oscillations generated by the HF generator 22 reach the coil 20 and are irradiated by the latter. Due to inductive coupling the resonance circuit 12 tuned to the frequency of the carrier oscillation is stimulated to oscillate. By means of the diode 26 the oscillations are subjected to a half-wave rectification and as a result the capacitor 28 is charged to half the amplitude of the carrier oscillation. The energy stored in the capacitor 28 is used as supply energy for the rest of the circuit as soon as the carrier oscillation ceases after opening of the switch 24.

The amplitude detector circuit 44 detects both the start of the carrier oscillation and the end thereof. An example of the makeup of such an amplitude detector circuit is shown in Fig. 2. The corresponding description will follow later.

As long as the carrier oscillation is emitted by the transmitter 18 and the capacitor 28 is fully charged the supply voltag at the supply voltage line 32 does not drop but remains constant. The amplitude detector circuit which reacts to a reduction of the amplitude of the oscillations present at the resonance circuit 12 furnishes in this case a signal with a low value at its output 42 which results in a signal with low value being present at the gate electrode of the MOS field-effect transistor T2 as well so that said transistor is kept nonconductive. Since the input of the negator 68 is held via the resistor 66 at the supply voltage value and the output of said negator 68 and thus also the gate electrode of the MOS field-effect transistor T1 is connected to ground via the resistor 70, said transistor is likewise nonconductive and this means that the resonance circuit 12 is practically separated from the rest of the circuit so that in the charging phase of the capacitor 28 no current is consumed by the rest of the circuit, apart from leakage currents. The energy transmitted by the transmitter 18 and received by the resonance circuit 12 is thus used in optimum manner for building up the voltage at the capacitor 28.

After a predefined period of time the switch 24 is opened so that no more carrier oscillations can be received by the resonance circuit 12. The oscillations of the resonance circuit therefore become smaller in amplitude and in accordance with the quality of the resonance circuit they would approach zero aperiodically at a greater or lesser rate if the effect of the remaining components and assemblies in the circuit arrangement 10 did not occur. The amplitude detector circuit 44, which is connected via the input 50 to the resonance circuit 12 and via the input 46 to the supply voltage line 32, detects that the oscillation amplitude starts to drop with respect to the supply voltage value at the supply voltage line 32. As reaction to this detection the amplitude detector circuit 44 furnishes at its output 42 a signal with the value "1" which passes to the input of the AND circuit 40. Since at the other input of said AND circuit 40 the supply voltage is present, representing the signal value "1", a high signal value also appears at the output of the AND circuit 40 and leads to the MOS field-effect transistor T2 becoming conductive. The MOS field-effect transistor T2 therefore switches the negative half-waves of the oscillations of the resonance circuit 12 through to the input of the negator 34 which exerts a certain limiting effect on said half-waves so that at its output an approximately rectangular pulse-like signal appears which is supplied to the output 72 of the circuit arrangement 10 and in further circuit units not illustrated can be used as clock signal. In addition, the signal passes from the output of the negator 34 via the negator 52 to the input of the NOR circuit 54 and to the counting input 56 of the counter 58. Said counter 58 is set so that after receiving a predetermined number of pulses at the counting input 56 it furnishes at its output 60 a pulse which by logic combination with

field-effect transistor T3 begins to rise. This transistor is therefore moved to the conductive state and as a result at the setting input 84 of the flip-flop a signal with low voltage value appears. The setting input 84 of the flip-flop is formed so that it reacts to the application of a signal with low value and effects switching over of the flip-flop 86 to the set state. As a result, at the output 42 of the amplitude detector circuit 44 a signal with high value appears and passes to the AND circuit 40. Said AND circuit thereupon likewise furnishes at its output a signal with high value which renders the MOS field-effect transistor T2 conductive. Thus, the amplitude detector circuit furnishes both at the start of the HF oscillation circuit and at the end thereof a definite output signal at the output 42 which is used in the manner described above for controlling the generation of the stimulation pulses for the resonance circuit 12.

Claims

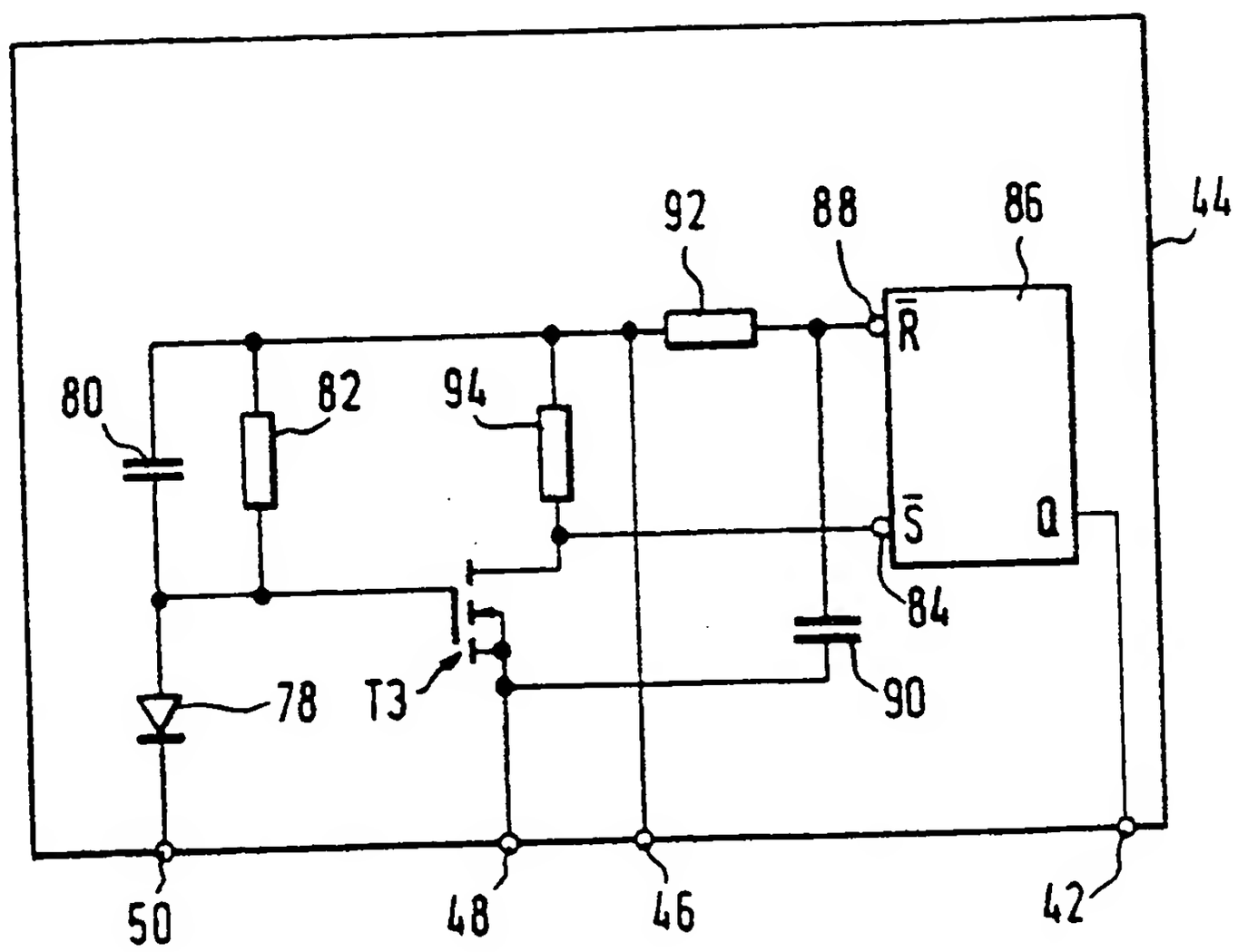
1. Circuit arrangement for generating pulses for maintaining the oscillations of a resonance circuit after termination of an outside excitation of the oscillations by means of an HF carrier oscillation, characterized by an energy storage element (28) chargeable by the HF carrier oscillation to a supply voltage value, an amplitude detector circuit (44) for generating a trigger signal when the oscillation amplitude of the resonance circuit (12) drops below the supply voltage value, a first switching element (T2) which under the control of the trigger signal supplies the oscillations of the resonance circuit (12) to a delay circuit which furnishes at its output switching pulses having a predetermined phase position with respect to the oscillations of the resonance circuit (12), and a second switching element (T1) which for the duration of each switching pulse enables the supply of energy from the energy storage element (28) to the resonance circuit (12).

2. Circuit arrangement according to claim 1, characterized in that the delay circuit (34, 52, 58, 54, 62, 68) comprises a counter (58) which after receiving a predetermined number of advancing pulses derived from the oscillation signal of the resonance circuit (12) furnishes an enable signal.

3. Circuit arrangement according to claim 2, characterized in that the delay circuit comprises a plurality of series connected delay members (34, 52, 58, 54, 62, 68) and that the counter (58) is one of the delay members.

4. Circuit arrangement according to claim 1, 2 or 3, characterized in that the amplitude detector circuit (44) includes a flip-flop (86) which from an evaluation circuit receives a setting signal when the oscillation amplitude of the resonance circuit drops and that the flip-flop (86) furnishes the trigger signal in the set state.

FIG.2



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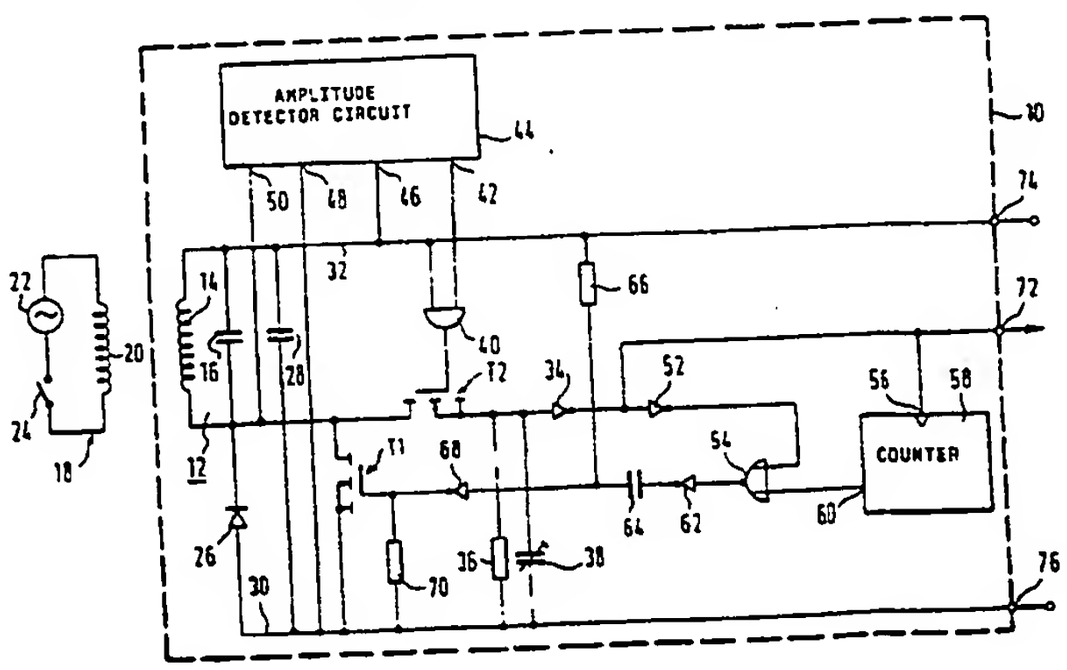

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